ECE 463: Microprocessor Architecture

In Workflow
1. 14ECE UG Director of Curriculum (mjescuti@ncsu.edu; jtuck@ncsu.edu)
2. 14ECE GR Director of Curriculum (dgyu@eos.ncsu.edu; paulf@ncsu.edu)
3. 14ECE UnderGrad Head (ddstanci@ncsu.edu; gbyrd@ncsu.edu)
4. COE CC Coordinator UG (amy_matthews@ncsu.edu; dwparish@ncsu.edu)
5. COE CC Meeting UG (All)
6. COE CC Chair UG (All)
7. COE Final Review UG (amy_matthews@ncsu.edu)
8. COE Dean UG (jerome_lavelle@ncsu.edu)
9. COE CC Coordinator GR (rfillin@ncsu.edu)
10. COE CC Chair GR (john_classen@ncsu.edu)
11. COE Final Review GR (rfillin@ncsu.edu)
12. COE Dean GR (reeves@csc.ncsu.edu)
13. OUCC Review (courses-curricula@ncsu.edu, aeherget@ncsu.edu, lamarcus@ncsu.edu)
14. UCCC Coordinator (courses-curricula@ncsu.edu, aeherget@ncsu.edu, lamarcus@ncsu.edu)
15. UCCC Meeting (courses-curricula@ncsu.edu, aeherget@ncsu.edu, lamarcus@ncsu.edu)
16. mdlewis (mdlewis@ncsu.edu)
17. anmatthe (amy_matthews@ncsu.edu)
18. OUCC Review (courses-curricula@ncsu.edu, aeherget@ncsu.edu, lamarcus@ncsu.edu)
19. UCCC Chair (andy_nowel@ncsu.edu)
20. OUCC Final Signature (barbara_kirby@ncsu.edu)
21. OUCC Final Review (lamarcus@ncsu.edu)
22. ABGS Coordinator (george_hodge@ncsu.edu; lian_lynch@ncsu.edu; mlnosbis@ncsu.edu)
23. ABGS Meeting (george_hodge@ncsu.edu; lian_lynch@ncsu.edu; mlnosbis@ncsu.edu)
24. ABGS Chair (george_hodge@ncsu.edu; lian_lynch@ncsu.edu; mlnosbis@ncsu.edu)
25. Grad Final Review (george_hodge@ncsu.edu; lian_lynch@ncsu.edu; mlnosbis@ncsu.edu)
26. PeopleSoft (none)

Approval Path
1. Mon, 15 Feb 2016 20:29:38 GMT
   James Tuck (jtuck): Approved for 14ECE UG Director of Curriculum
2. Thu, 18 Feb 2016 18:58:05 GMT
   Donna Yu (dgyu): Approved for 14ECE GR Director of Curriculum
3. Thu, 18 Feb 2016 19:14:34 GMT
   Gregory Byrd (gbyrd): Approved for 14ECE UnderGrad Head
   David Parish (dwparish): Approved for COE CC Coordinator UG
5. Wed, 06 Apr 2016 16:05:43 GMT
   David Parish (dwparish): Approved for COE CC Meeting UG
   David Parish (dwparish): Approved for COE CC Chair UG
7. Wed, 06 Apr 2016 21:09:52 GMT
   David Parish (dwparish): Approved for COE Final Review UG
8. Fri, 08 Apr 2016 15:05:50 GMT
   Jerome Lavelle (jerome_lavelle): Approved for COE Dean UG
9. Fri, 08 Apr 2016 15:52:52 GMT
   Robyn Fillinger (rfillin): Approved for COE CC Coordinator GR
10. Fri, 08 Apr 2016 18:04:48 GMT
    Mihail Devetsikioti (mdevets): Approved for COE CC Chair GR
11. Fri, 08 Apr 2016 18:06:04 GMT
Date Submitted: Mon, 15 Feb 2016 20:28:26 GMT

Viewing: ECE 463/ECE 563: Microprocessor Architecture

Changes proposed by: jtuck

Change Type
Major

Course Prefix
ECE (Electrical and Computer Engineering)

Course Number
463
Course ID
006059

Dual-Level Course
Yes

Dual-Level Course Number:
563

Cross-listed Course
No

Title
Microprocessor Architecture

Abbreviated Title
Microarch

College
College of Engineering

Academic Org Code
Electrical & Computer Engineering (14ECE)

CIP Discipline Specialty Number
14.1001

CIP Discipline Specialty Title
Electrical and Electronics Engineering

Term Offering
Fall and Spring

Year Offering
Offered Every Year

Effective Date
Spring 2016

Previously taught as Special Topics?
No

Course Delivery
Face-to-Face (On Campus)

Grading Method
Graded with S/U option

Credit Hours
3

Course Length
16
weeks

Contact Hours
(Per Week)

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Contact Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lecture</td>
<td>3.0</td>
</tr>
</tbody>
</table>

Course Attribute(s)

Course Is Repeatable for Credit
No

Instructor Name
Eric Rotenberg

Instructor Title
Professor

Grad Faculty Status
Full

Anticipated On-Campus Enrollment
Open when course_delivery = campus OR course_delivery = blended OR course_delivery = flip

<table>
<thead>
<tr>
<th>Enrollment Component</th>
<th>Per Semester</th>
<th>Per Section</th>
<th>Multiple Sections?</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lecture</td>
<td>1</td>
<td>100</td>
<td>No</td>
<td>Combined 463/563 section..</td>
</tr>
</tbody>
</table>

Course Prerequisites, Corequisites, and Restrictive Statement

463 prerequisites: ECE 209 and ECE 212
563 prerequisites: Graduate Standing

Is the course required or an elective for a Curriculum?
Yes

Which Curricula are Affected?

<table>
<thead>
<tr>
<th>SIS Program Code</th>
<th>Program Title</th>
<th>Required or Elective?</th>
</tr>
</thead>
<tbody>
<tr>
<td>14CPBES</td>
<td>Computer Engineering</td>
<td>Elective</td>
</tr>
<tr>
<td>14EEBS</td>
<td>Electrical Engineering</td>
<td>Elective</td>
</tr>
</tbody>
</table>

Catalog Description

Architecture of microprocessors. Measuring performance. Instruction-set architectures. Memory hierarchies, including caches, prefetching, program transformations for optimizing caches, and virtual memory. Processor architecture, including pipelining, hazards, branch prediction, static and dynamic scheduling, instruction-level parallelism, superscalar, and VLIW. Major projects.

Justification for each revision:

1. Title and Abbreviated title change.

The new title better conveys the course's content. Microprocessor architecture is a term with a narrower and more specific meaning, pertaining directly to the design of the logic and overall organization of microprocessors. The older title is broader and possibly misleading to students and other stakeholders.

The new abbreviation better matches the new title.

2. Prerequisites:

The proposed change is to add ECE 209 and 212 as the prerequisite. ECE 209 covers programming with data structures and the C programming language. Substantial prior programming experience is required for this course because students implement simulators of computer architecture
components. While ECE 209 is already required for both CPE and EE students, currently, there is nothing preventing students from taking ECE 463 before ECE 209. Making ECE 209 a prerequisite of ECE 463 enforces the correct course sequence.

ECE 212 is required for the basics of digital systems design. ECE 310 (formerly 406 and listed as a prerequisite) could be selected instead of 212, but the more advanced material covered in 310 is not strictly required for the material in this course.

3. Catalog description:
The current catalog description is outdated. For example, ECE 463 is primarily concerned about uniprocessor design and not multiprocessor design, so reference to the latter has been removed. On the other hand, the enumeration of processor topics has been made more descriptive and comprehensive.

4. Content:
Processor technology evolves rapidly and semiconductor technology trends cause emphasis to shift from one performance metric to another (for example, power consumption, cycle time, etc.). Faculty in charge of ECE 463 continuously update the content of the course accordingly. Note that the fundamental content has not changed.

Rather, certain outdated aspects receive less emphasis, certain other aspects receive more emphasis (e.g., virtual memory, critical paths and cycle time impact, etc.), and new aspects are introduced (e.g., modeling energy consumption in projects).

5. Student learning outcomes:
Student learning outcomes are described more comprehensively and in more depth. This is a result of continuous assessment consistent with ABET goals.

6. Dual Level Listing
463 and 521 are currently co-taught as a dual listed course sequence. Under new rules, the dual listed course must be numbered 563. So, we will add that as a new course and later drop 521.

The difference in requirements between 463 and 563 are enumerated in the Student Evaluation Methods. There are two main differences: (1) projects for 463 have substantially reduced scope compared to 563, and (2) the midterm and final exam have additional questions for 563 students that demand greater or deeper mastery of the material.

Does this course have a fee?
No

Is this a GEP Course?
No

Consultation

Instructional Resources Statement
No additional resources are needed.

Course Objectives/Goals
This course covers the architecture of high-performance processors and memory systems. Students undertake three major architecture simulation projects.

Student Learning Outcomes
1. Describe techniques for quantifying or measuring the performance of a microprocessor (CPU) when running a workload.

2. Define Instruction-Set Architecture (ISA) and what it specifies. This includes explaining its importance, distinguishing between software, ISA, and hardware, describing important historical trends, and designing ISA features.

3. Describe the rationale and structure of high performance cache memory hierarchies, and explain the role of temporal and spatial locality of data in their design.

4. Explain the importance of Virtual Memory, and describe the architectural mechanisms that support it.

5. Explain how a pipelined processor executes instructions; analyze and identify common pipeline hazards; and, describe techniques for mitigating them.
6. Explain the meaning of superscalar processing and describe multiple architectural approaches for supporting it; also, characterize the performance
differences and the logic complexity of superscalar processing compared with scalar processing.

7. Apply knowledge from prior objectives to simulate microprocessors and their components both manually and by constructing software programs that
perform the simulation.

8. Design microarchitectural components, and use simulation to measure performance and evaluate alternative microarchitectural designs.

**Student Evaluation Methods**

<table>
<thead>
<tr>
<th>Evaluation Method</th>
<th>Weighting/Points for Each</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>10%</td>
<td>There will be approximately 4 to 6 homeworks throughout the semester, covering major topics: measuring performance, caches and memory hierarchies, ISAs and pipelining, and instruction-level parallelism.</td>
</tr>
<tr>
<td>Project</td>
<td>15%</td>
<td>Project 1. Typically, the first project involves (1) constructing a cache and memory hierarchy simulator with various optimizations and flexible parameters, and (2) extensive design space exploration of the optimal memory hierarchy for each benchmark program, in terms of various performance, cost, and power metrics. ECE 563 students are required to implement and evaluate more design features. The project for 563 students is more challenging and of significantly greater scope.</td>
</tr>
<tr>
<td>Project</td>
<td>10%</td>
<td>Project 2. Typically, the second project involves (1) constructing a dynamic branch predictor simulator with various optimizations and flexible parameters, and (2) extensive design space exploration of the optimal dynamic branch predictor for each benchmark program in terms of various performance, cost, and power metrics. ECE 563 students are required to implement and evaluate more design features. The project for 563 students is more challenging and of significantly greater scope.</td>
</tr>
<tr>
<td>Project</td>
<td>15%</td>
<td>Typically, the third project involves (1) constructing a Tomasulo-style pipeline simulator with various optimizations and flexible microarchitectural parameters, and (2) extensive characterization of performance as a function of key microarchitectural parameters. ECE 563 students are required to implement and evaluate more design features. The project for 563 students is more challenging and of significantly greater scope.</td>
</tr>
<tr>
<td>Midterm</td>
<td>25%</td>
<td>The midterm exam covers the first half of the semester which typically includes the following major units: measuring performance, caches and memory hierarchies, and instruction-set architectures. ECE 563 students are given additional questions that evaluate mastery of material at a deeper level.</td>
</tr>
</tbody>
</table>
Final Exam 25%

The final exam may be comprehensive or may cover only the second half of the semester, at the discretion of the instructor. The second half of the semester typically includes the following major units: pipelining and instruction-level parallelism.

ECE 563 students are given additional questions that evaluate mastery of material at a deeper level.

Topical Outline/Course Schedule

Syllabus

ECE_463_and_563_001update.pdf

Additional Documentation

Additional Comments

The syllabus includes a detailed schedule so it is not replicated above.

minosbis 10/19/2016: No overlapping courses. MAE 534 mentions microprocessor architecture as a topic, but College of Engineering has fully approved this course, indicating no overlapping content.

ghodge 10/20/2016 ready for ABGS reviewers

ABGS Reviewer Comments:
-None

Course Reviewer Comments

svhoward (Thu, 21 Apr 2016 12:10:08 GMT): svhoward: updated to “not repeatable for credit” with instructor permission
aehlerget (Tue, 16 Aug 2016 18:12:27 GMT): AECHH: Confirmed prerequisites by Dr. David Parish 8/15/2016 via email.
aehlerget (Fri, 09 Sep 2016 18:06:23 GMT): Rollback: AECHH: Syllabus needs to be updated. Prerequisites in syllabus need to match CIM. Student Learning Outcomes in syllabus need to match CIM. Disabilities Statement in syllabus must match the statement from https://policies.ncsu.edu/regulation/reg-02-20-07 9/9/2016

Key: 1756